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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,051	11/07/2001	Nobuyoshi Aways	900-403	4813
23117	7590	10/24/2003	EXAMINER	
NIXON & VANDERHYE, PC 1100 N GLEBE ROAD 8TH FLOOR ARLINGTON, VA 22201-4714			NGUYEN, HA T	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 10/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/986,051

Applicant(s)

AWAYA, NOBUYOSHI

Examiner

Ha T. Nguyen

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5, 10 and 11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 10 and 11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s): \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other:

## **DETAILED ACTION**

### ***Notice to applicant***

1. Applicant's Amendment and Response to the Office Action mailed 3-14-3 and Request for a Continued Examination have been entered and made of record (Paper No. 10 and 0603). Following is an Office Action responding to the request.

### ***Response to Amendment***

2. In view of Applicant's arguments and the amendment to the claims, the rejections of claims 1-5 under 35 U.S.C. 102 or 103, as stated in Paper No. 9, have been withdrawn.

Applicant's arguments with regard to the rejections under 35 U.S.C. have been fully considered, but they are not deemed to be persuasive. The response to these arguments will be incorporated in the new ground of rejection given below.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ball et al. (USPN 6246112, hereinafter "Ball") in view of Kitazawa et al. (USPN 5952709, hereinafter "Kitazawa")

Referring to Figs. 1-8 and related text, Ball discloses a semiconductor device comprising: regions for forming a plurality of functional blocks 62, 64; and a region for forming wiring layers 68 for connecting the functional blocks; wherein each of the regions for forming the functional blocks includes a multilayer wiring (see Figs 3, 4), and wherein the region for forming the wiring layers for connecting adjacent functional blocks includes transmission line comprising a signal line and ground lines and/or power source lines formed above and below the

signal line, respectively, as viewed cross sectionally, to sandwich the signal line via an insulating film (see par. bridging cols. 2 and 3). It also discloses that the device is used in transmitting high speed signals (see col. 3, lines 50-67).

But it does not disclose expressly the frequency used is in the GHz range.

However, the missing limitation is well known in the art because Kitazawa discloses this features (See Example 2).

A person of ordinary skill is motivated to modify Ball with Kitazawa to have the device used in high frequency applications.

[Claim 11] It is well known in the art that the cross section of a wiring determine the flow and speed of current or signal transmitted through the wiring. It would have been obvious to have the thickness of the inner signal line of the coaxial line larger than the one for wiring layers in the functional blocks.

Therefore, it would have been obvious to combine Ball with Kitazawa to obtain the invention as specified in claims 3 and 11.

5. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ball in view of Kitazawa and Sim et al. (USPN 6242796, hereinafter "Sim") and Kitazawa.

Referring to Figs. 1-8 and related text, Ball discloses a semiconductor device comprising: regions for forming a plurality of functional blocks 62, 64; and a region for forming wiring layers 68 for connecting the functional blocks; wherein each of the regions for forming the functional blocks includes a multilayer wiring (see Figs 3, 4), and wherein the region for forming the wiring layers for connecting adjacent functional blocks includes transmission line comprising a signal line and ground lines or power source lines formed above and below the signal line, respectively to sandwich the signal line via an insulating film, via an insulating film as viewed cross sectionally. It also discloses that the device is used in transmitting high speed signals (see col. 3, lines 50-67).

But it does not disclose expressly a coaxial line comprising an inner signal line and an outer ground line surrounding the signal line and that the frequency used is in the GHz range.

However, the missing limitation is well known in the art because Kitazawa (as shown above) and Sim discloses these features (See Sim, abstract and Fig. 5).

A person of ordinary skill is motivated to modify Ball with Sim to reduce distortion of transmitted signal (see Sim, Summary). Note that both Ball and Sim address the wiring feature of a semiconductive device they are combinable. A semiconductive device is a broad term, it may include more than one chip.

[Claim 10] Arguments used for the rejection of claim 11 also applies.

Therefore, it would have been obvious to combine Ball with Sim and Kitazawa to obtain the invention as specified in claims 1 and 10.

6. Claims 2, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ball in view of Kitazawa or Ball in view of Sim and Kitazawa and further in view of Parikh (U.S. Patent 6225207).

The combined teaching of Ball and Kitazawa or Ball, Kitazawa and Sim discloses substantially the limitations of claims 2, 4, and 5, as shown above.

But it does not disclose expressly wherein a bottom surface of a wiring in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the ground line or power source line located below the transmission line provided in the region for forming the wiring layers for connecting the functional blocks.

However, the missing limitation is well known in the art because Parikh discloses in various embodiment the simultaneous formation of power and signal wiring for different levels including for example power line 1042 and signal line 1046 in Fig. 10D, they have bottom surface on the same plane. Besides, it would have been obvious for a person of ordinary skill in the art to use thicker wiring layers in the region for forming wiring layers than in the functional blocks to increase transmission speed.

A person of ordinary skill is motivated to modify Ball and Kitazawa or Ball, Kitazawa and Sim with Parikh to obtain a simplified process ensuring a reduction in production cost of device made.

Therefore, it would have been obvious to combine Ball and Kitazawa or Ball, Kitazawa, and Sim with Parikh to obtain the invention as specified in claims 2, 4, and 5.

*Conclusion*

7. The prior art relevant to the disclosure of this application and not being used in the rejections.

USPN 6481013 to Dinwiddie et al. and USPAPN 2002/0030628 to Tsai for teaching the use of wiring in applications for high frequency signals.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha Nguyen whose telephone number is (703)308-2706 . The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week. The phone number for Wednesday is (703) 560-0528.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (703) 308-3325. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.



Ha Nguyen  
Primary Examiner  
10- 17- 03